Interconnects

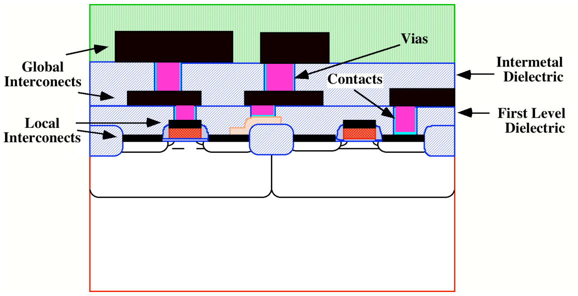
Outline

- Interconnect scaling issues
- Aluminum technology
- Copper technology

Properties of Interconnect Materials

	Material	Thin film resistivity ($\mu\Omega - cm$)	Melting point (˚C)
Metals	Cu	1.7-2.0	1084
	Al	2.7-3.0	660
	W	8-15	3410
Silicides	PtSi	28-35	1229
	$TiSi_2$	13-16	1540
	WSi_2	30-70	2165
	$CoSi_2$	15-20	1326
	NiSi	14-20	992
Barriers	TiN	50-150	~2950
	$Ti_{30}W_{70}$	75-200	~2200
	N+ polysilicon	500-1000	1410

Interconnect Architecture



- **SILICIDES - Short local interconnections which have to be exposed to high temperatures and oxidizing ambients, e.g., polycide and salicide structures.**
- **REFRACTORY METALS – Via plugs, future gate electrodes, local interconnections which need very high electromigration resistance.**
- **TiN, TiW – Barriers, glue layers, anti reflection coatings and short local interconnections.**
- **Al, Cu - for majority of the interconnects**

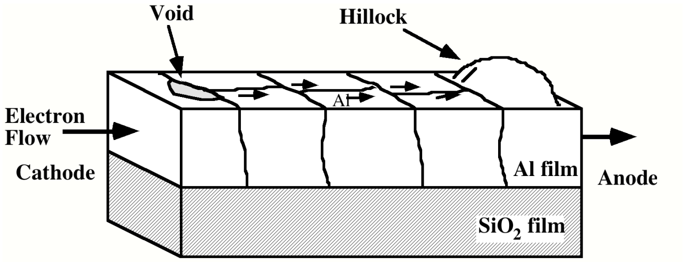
Why Aluminum?

Al has been used widely in the past and is still used

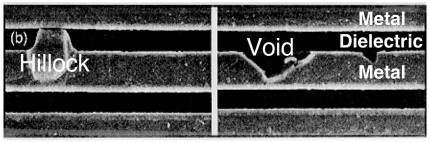
✓ Low resistivity
✓ Ease of deposition,
✓ Dry etching
✓ Does not contaminate Si
✓ Ohmic contacts to Si but problem with shallow junctions
✓ Excellent adhesion to dielectrics
☹ Problems with Al
  - Electromigration ⇒ lower life time
  - Hillocks ⇒ shorts between levels
  - Higher resistivity

Electromigration

Electromigration induced hillocks and voids



Electromigration due to electron wind induced diffusion of Al through grain boundaries



SEM of hillock and voids formation due to electromigration in an Al line

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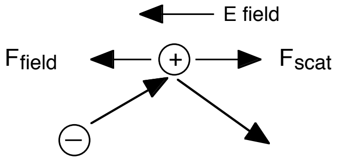
Electromigration Theory



$$F_{TOTAL} = F_{SCAT} + F_{FIELD}$$

$$\cong qz^{*}\vec{E}$$ Where qz* is effective ion charge

$$\upsilon_D = \mu\,\vec{E} = \frac{qZ^*}{kT}\cdot D\cdot\vec{E}$$ Using Einstein's relation

current density is related to E field by $J = \sigma\vec{E} = \frac{\vec{E}}{\rho}$

Diffusivity is given by $D = D_o\,e^{-\frac{Ea}{kT}}$

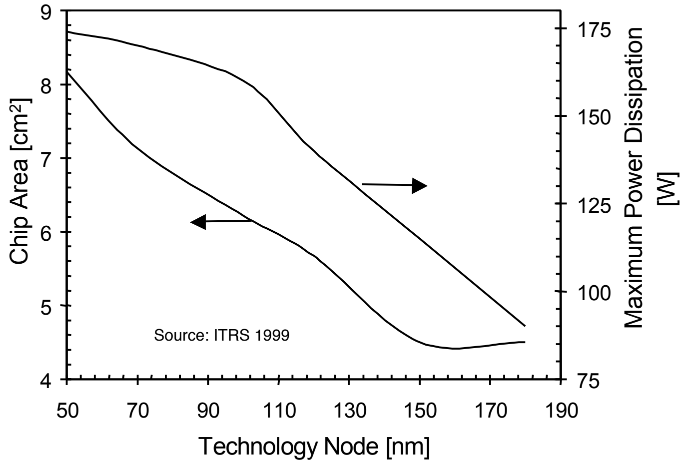
Therefore $\upsilon_D = J\,\rho\,\frac{qZ^*}{kT}D_0\,e^{-\frac{E_a}{kT}}$

Meantime to failure is thus of the form of $MTF \propto e^{Ea/kT}$

A phenomenological model for MTF is $MTF = \frac{A}{\gamma^m J^n}\,e^{Ea/kT}$

γ is the duty factor
M, n are constants

Thermal Behavior in ICs

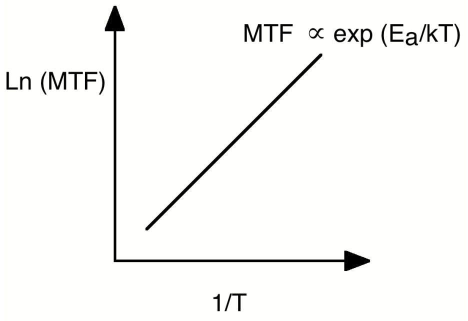


Source: ITRS 1999

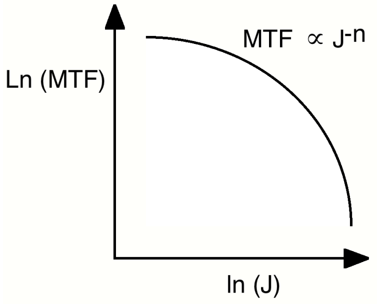
- Energy dissipated is increasing as performance improves
- Average chip temperature is rising

Parametric Dependencies of Electromigration

Temperature



Current Density



Mean time to failure is $$MTF = \frac{A}{r^m J^n} \exp\left(\frac{E_a}{kT}\right)$$

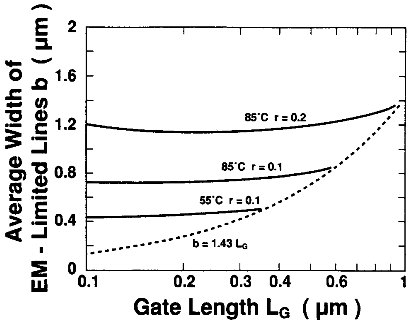
r **is duty cycle**
J **is current density**
E_a is activation energy
T **is temperature**
A, m, **and** ***n*** **are materials related constants**

Electromigration-Induced Integration Limits

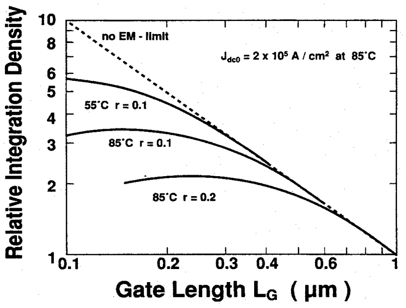
$$MTF = \frac{A}{r^m J^n} \exp\left(\frac{E_a}{kT}\right)$$

r = duty cycle
J =current density

EM Limited Interconnect Width



EM Limited Device Integration Density



Ref: Yi, et al., IEEE Trans. Electron Dev., April 1995

Better packing techniques will be needed in the future to minimize the chip temperature rise

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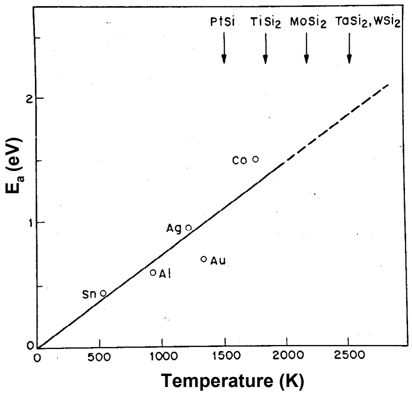
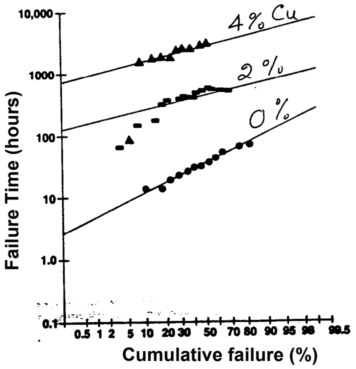
Electromigration: Material and Composition

Materials



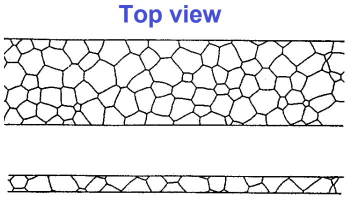
Materials with higher activation energy have higher resistance to electromigration

Composition

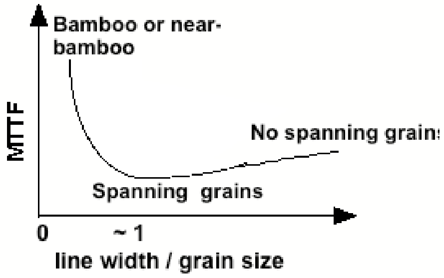


Adding Cu to Al decreases its self diffusivity and thus increases resistance to electromigration

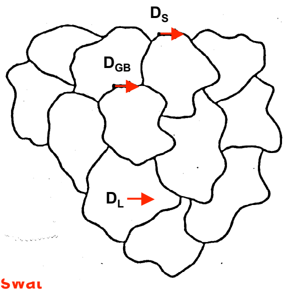
Electromigration: Grain Structure



Near bamboo structure



Self Diffusion in Polycrystalline Materials



- For Al grain boundary diffusion $D_{GB} >> D_s$ or D_L (D_s = surface diffusion, D_L = lattice diffusion)
- In a bamboo structure grain boundary diffusion is minimized

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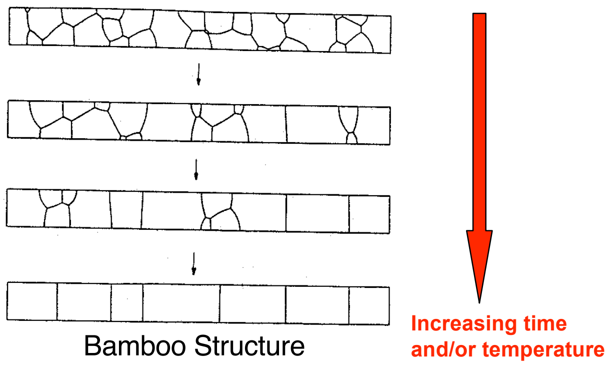
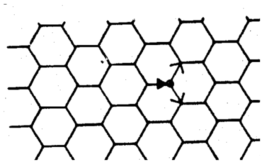
Effect of Post Patterning Annealing on the Grain Structure of the Film.



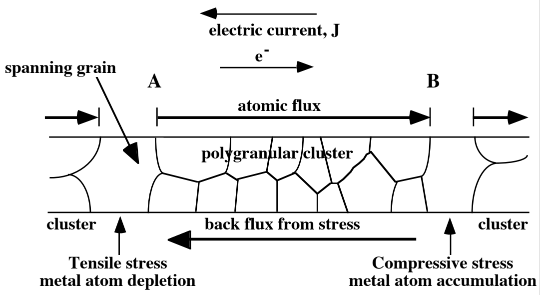
- *With sufficient grain boundary migration a "bamboo structure" may develop*
- *No grain boundary diffusion in the bamboo structure*

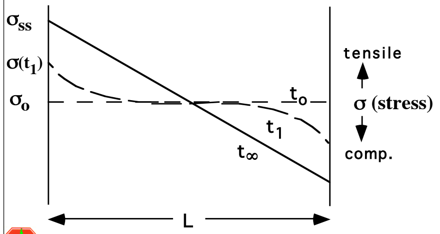
Microstructural Inhomogeneities and Stress Induced Electromigration

On an average the flux is uniform in a uniform grain size textured film.



If the grain size is non uniform the flux will vary accordingly.


electric current, J
e^-
spanning grain
A
B
atomic flux
polygranular cluster
cluster
back flux from stress
cluster
Tensile stress
metal atom depletion
Compressive stress
metal atom accumulation



build up of stress within polygranular cluster with time due to electromigration

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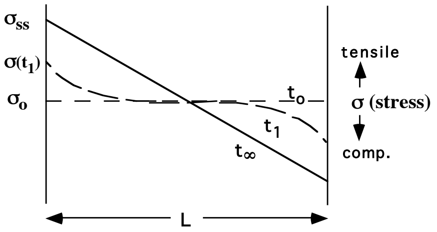
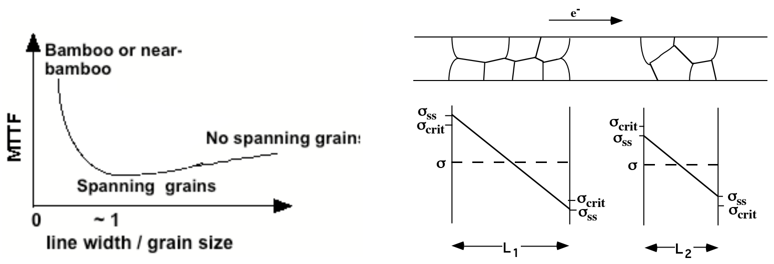
Build up of stress within polygranular cluster with time due to electromigration.



- Eventually, a steady-state is approached where the forward flux is equal to the backward flux due to stress.
- A criterion for failure of an interconnect under electromigration conditions could be if the steady-state stress is equal to or greater than some critical stress for plastic deformation, encapsulent rupture, large void formation, etc.
- The maximum steady state stress would occur at x=0 or x=L



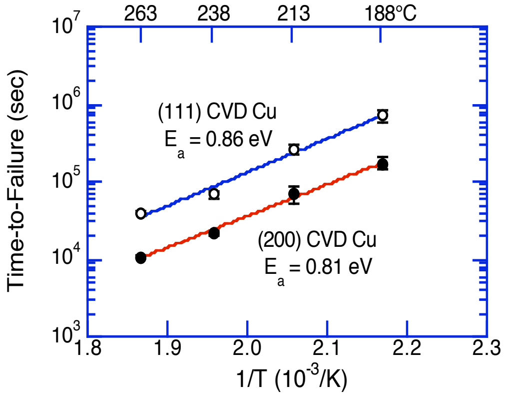
- For very large line width/grain size (w/d) values, no spanning grains are present. No points of flux divergence are present and the time to failure is relatively high.
- As w/d decreases, some spanning grains occur. This results in divergences in the flux, causing stress to develop that can be greater than the critical stress for failure (with L > L_{crit} for most or all of the polygranular clusters). The lines would fail and the median time to failure would decrease.
- As w/d decreases more, more spanning grains are present, but the lengths of the polygranular cluster regions between them are shorter, many of them shorter than L_{crit}. The stresses that develop, which create the back fluxes and which in turn eventually stop the electromigration flux, are in many cases smaller than the critical stress.
- For small enough values of w/d bamboo or near-bamboo structures are present. The polygranular clusters are few, and for some lines, all the clusters are shorter than L_{crit} and the lines will not fail by this mechanism. The MTTF thus increases dramatically.

Electromigration: Grain Texture

- Empirical relationship (for Al & Al alloys)

$$MTF \propto \frac{e^{\mu}}{\sigma^2}\log\left[\frac{I_{(111)}}{I_{(200)}}\right]^3$$

S. Vaidya et al., Thin Solid Films, Vol. 75, 253, 1981

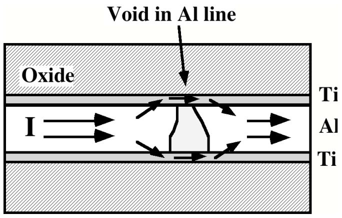


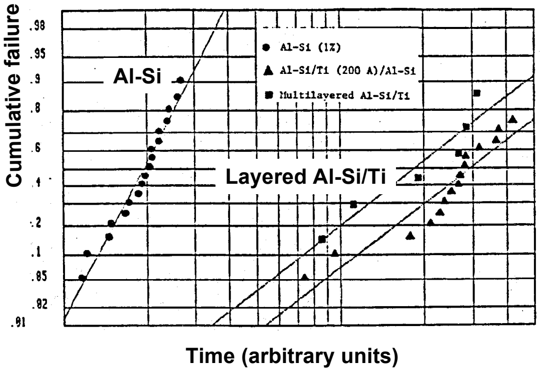
Ref: Ryu, Loke, Nogami and Wong, IEEE IRPS 1997.

Layered Structures: Electromigration

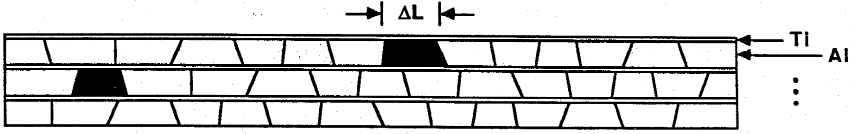
Layering with Ti reduces Electromigration

Structure





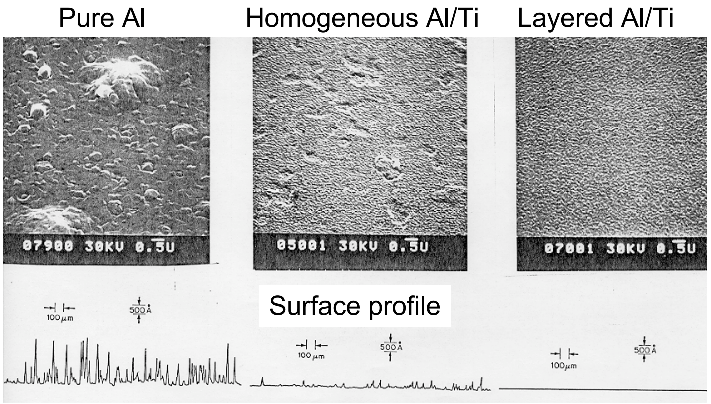
Improvements in layered films due to redundancy



Mechanical properties of interconnect materials

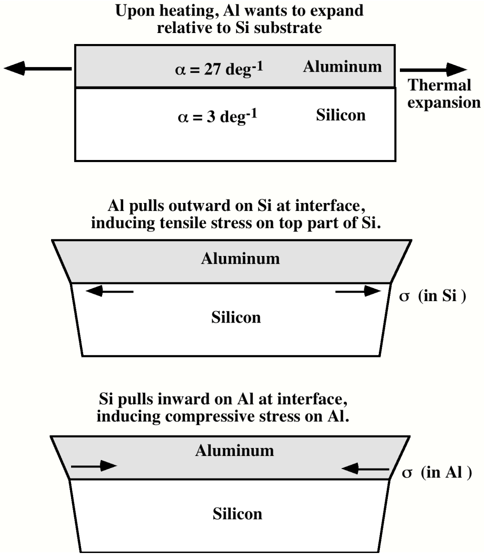
Material	Thermal expansion coefficient (1/˚C)	Elastic modulus, Y/(1-ν) (MPa)	Hardness (kg/mm2)	Melting point (˚C)
Al (111)	23.1×10^{-6}	1.143×10^{5}	19-22	660
Ti	8.41×10^{-6}	1.699×10^{5}	81-143	1660
$TiAl_3$	12.3×10^{-6}	-	660-750	1340
Si (100)	2.6×10^{-6}	1.805×10^{5}	-	1412
Si (111)	2.6×10^{-6}	2.290×10^{5}	-	1412
SiO_2	0.55×10^{-6}	0.83×10^{5}	-	~1700

Layered Structures: Hillocks



Layering with Ti reduces hillock formation

Stress due to Thermal Cycling



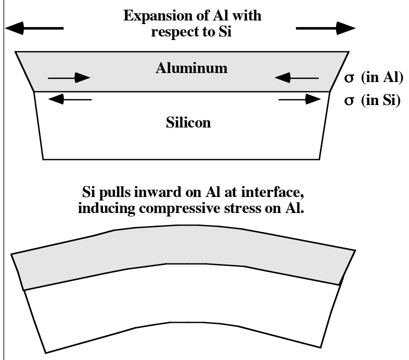
Difference in the expansion coefficients of the film and substrate causes stress in the thin film.

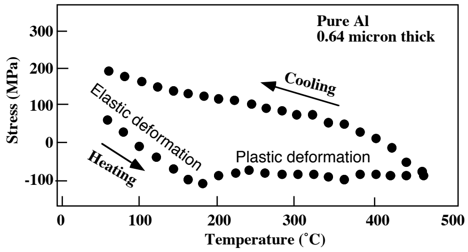
(a) Film as-deposited (stress free).

(b) Expansion of the film and substrate with increasing temperature.

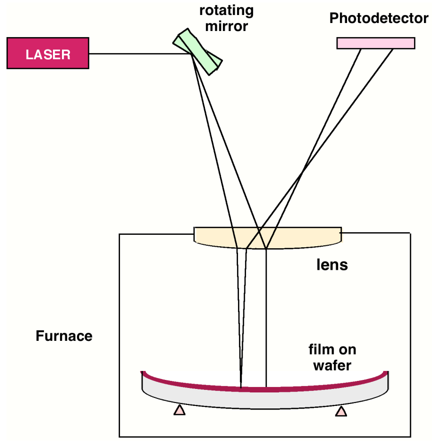
(c) Biaxial forces compress the Al film to the substrate dimension

Process Induced Stress





Stress Measurement

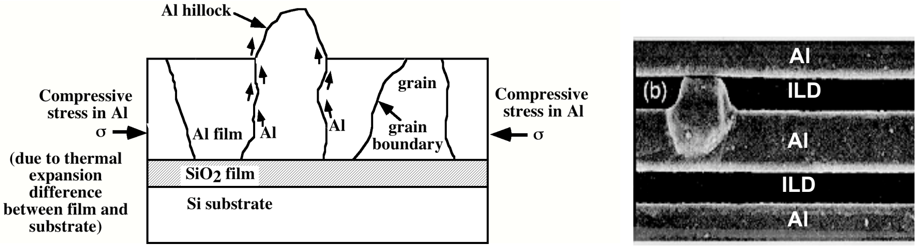


Biaxial stress in the film

$$\sigma = \left(\frac{E_s}{1-\nu_s}\right)\frac{t_s^2}{6t_fR_f}$$

- E_s is Young’s modulus of the substrate,
- v_s is Poisson’s ratio for the substrate,
- $(E_s/1-v_s)$ is the biaxial modulus of the substrate,
- t_s is the substrate thickness,
- t_f is the film thickness, and
- R_f is the radius of curvature induced by the film

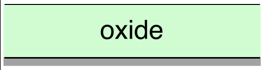
Hillocks



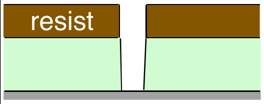
Hillock formation due to compressive stress and diffusion along grain boundaries in an Al film.

Current Aluminum Interconnect Technology

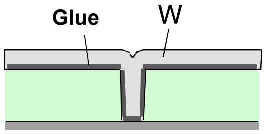
Fabrication of Vias



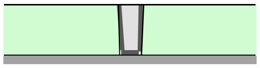
1. oxide deposition



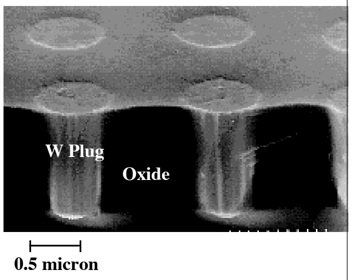
2. via etch



3. barrier & W fill

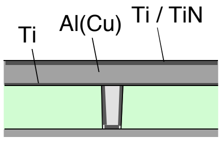


4. W & barrier polish

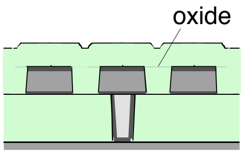


Current Aluminum Interconnect Technology

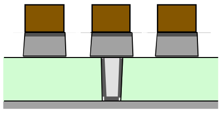
Fabrication of Lines



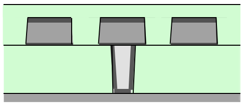
5. metal stack deposition



7. oxide gapfill

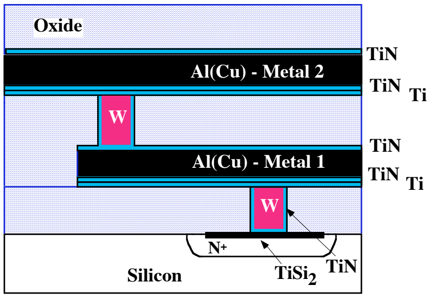


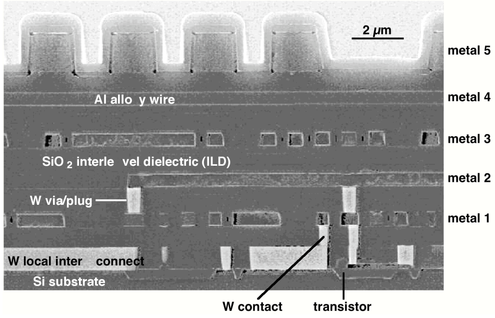
6. metal stack etch



8. oxide polish

Current Aluminum Interconnect Technology





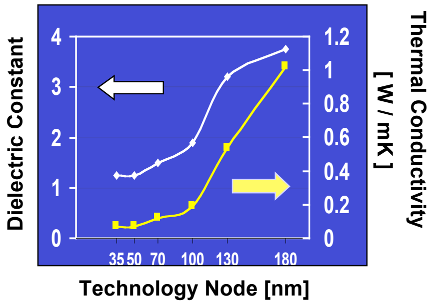
(Curtsey of Motorola)

Low Dielectric Constant (Low-k) Materials

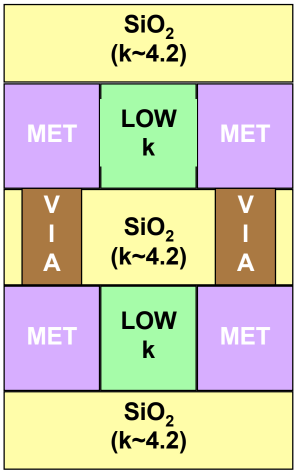
Oxide Derivatives	
F-doped oxides (CVD)	k = 3.3-3.9
C-doped oxides (SOG, CVD)	k = 2.8-3.5
H-doped oxides (SOG)	k = 2.5-3.3
Organics	
Polyimides (spin-on)	k = 3.0-4.0
Aromatic polymers (spin-on)	k = 2.6-3.2
Vapor-deposited parylene; parylene-F	k ~ 2.7; k ~ 2.3
F-doped amorphous carbon	k = 2.3-2.8
Teflon/PTFE (spin-on)	k = 1.9-2.1
Highly Porous Oxides	
Xerogels	k = 1.8-2.5
Air	k = 1

Thermal Conductivity for Commonly Used Dielectrics

Dielectric Film	Thermal Conductivity (mW/ cm°C)
HDP CVD Oxide	12.0
PETEOS	11.5
HSQ	3.7
SOP	2.4
Polyimide	2.4



Embedded Low-k Dielectric Approach

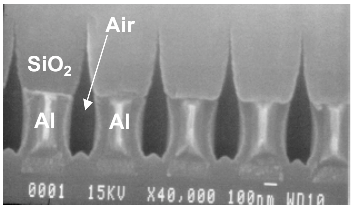


Source: Y. Nishi, TI

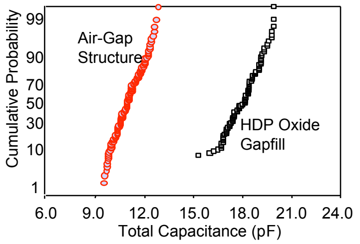
Why embed Low-k dielectric only between metal lines?

- Mechanical strength
- Moisture absorption in low-k
- Via poisoning/compatibility with conventional dry etch and clean-up processes
- CMP compatibility
- Ease of integration and cost
- Thermal conductivity

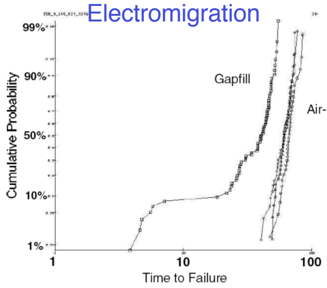
Air-Gap Dielectrics



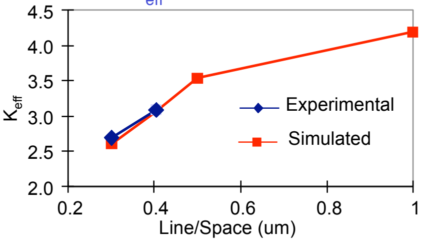
Capacitance



Electromigration



K_{eff} vs. Feature Size



- **Reduced capacitance between wires**
- **Heat carried mostly by the vias**
- **Electromogration reliability is better because of stress relexation allowed by free space**